IN THE BRIEF DESCRIPTION:

[0017] FIGUREs 1A to ~~1N~~ 1L illustrate sectional views of selected steps in a method of manufacturing a semiconductor device according to the principles of the present invention;

IN THE SPECIFICATION:

[0021] One embodiment of the present invention is a method of manufacturing a semiconductor device. FIGUREs 1A to ~~1N~~ 1L illustrate sectional views of selected steps in a method of manufacturing a semiconductor device 100, according to the principles of the present invention. Turning to FIGURE 1A, the method includes forming a gate dielectric 105 over a substrate 110. In some embodiments, it is advantageous to form isolation structures 112, via shallow trench isolation. As well understood by those skilled in the art, however, isolation structures 112 could be formed at any number of stages in the method.

[0025] The exemplary method continues as shown in FIGUREs ~~1M~~ 1K to ~~1N~~ 1L, with the fabrication of other semiconductor device components. As shown in FIGURE ~~1M~~ 1K, certain embodiments include removing portions of the first mold layer 115 (FIGURE 1G) or second mold layer 150 (FIGURE 1J), as well as portions of the gate dielectric layer 105 not under the first and second metal gate electrodes 125, 135. As further discussed below, in other embodiments, however, portions of the first or second mold layer 115, 150 can be retained to serve as part of an interconnect structure.

[0026] As presented in FIGURE ~~1N~~ 1L, certain embodiments of the method further include implanting dopants, with the metal gate electrodes 125, 135, serving as masks to facilitate forming source and drain structures 155, 160, and lightly doped drain regions 162, that are self-aligned with the first and second metal electrodes 125, 135. FIGURE ~~1N~~ 1L also illustrates forming sidewalls 165 adjacent to the first and second metals electrodes 125, 135. Other embodiments of the method further include, as illustrated in FIGURE ~~1N~~ 1L, the formation of NMOS and PMOS tubs, 170, 175.

[0027] With continuing reference to FIGUREs 1A-~~1N~~ 1L, the substrate 110 and gate dielectric 105 can be any conventional materials suitable for use in semiconductor device manufacturing, such silicon and silicon dioxide or silicon oxynitride, respectively. In certain preferred embodiments, the gate dielectric 105 is a high dielectric constant material (*e.g.*, a material having a higher dielectric constant than silicon dioxide), such as hafnium dioxide, hafnium silicate, hafnium silicon oxynitride or similar materials well known to those skilled in the art.

[0039] Yet another embodiment of the present invention, is an active device 200 produced by the processes described above and illustrated in FIGUREs 1A to ~~1N~~ 1L. FIGURE 2 illustrates a sectional view of an embodiment of an active device 200. Like reference numbers are used to depict structures analogous to that shown in FIGUREs 1A to ~~1N~~ 1L. With continuing reference to FIGUREs 1A to ~~1N~~ 1L, the active device 200 shown in FIGURE 2 is produced by a process that includes forming a gate dielectric 205 over a substrate 210 and depositing a mold layer 115 having a first opening 120 therein over the gate dielectric 205. Also included in the process is the creation of a first metal gate electrode 225 by depositing a first metal in the first opening 120.